in FIG. 6.

A clean version of the portion of the Specification is attached herewith.

In the Claims:

Please cancel Claim(s) 21.

Please amend the Claim(s) as follows:

Claim 1 (once amended):

1. [An] A universal testing module, capable of connecting to a computer having communication ports to be tested and forming communication paths through said ports, for testing the condition of each pin of a parallel port and a serial port of said communication ports, at least comprising:

a logic control unit, having at least a pair of input/output ports for communicating with said parallel port;

a memory unit for storing instructions for controlling said logic control unit and said computer and for temporary exchange of data; and an universal asynchronous receiver/transmitter; and

a voltage converter for voltage interchange of RS-232 and TTL and enabling said logic control unit to communicate with said computer through said serial port and executing said testing.

Claim 2 (once amended):

2. [An] A universal testing module according to claim 1 wherein said memory unit comprises:

an electrically erasable programmable read-only memory for storing machine code instructions for testing said communication port; and

a random-access memory for temporary exchange of data.

Claim 3 (once amended):

3. [An] A universal testing module according to claim 1 wherein said memory unit is located outside said logic control unit.

Claim 4 (once amended):

4. [An] A universal testing module according to claim 1 further comprising a clock circuit for providing time signals, and a reset circuit.

Claim 17 (once amended):

17. A universal testing module according to claim 1 wherein said logic control unit [for testing open condition of a parallel port of a computer, comprising] further comprises:

a first gate having a first data end, a first output end and a first control end;

a second gate having a second data end, a second output end and a second control end;

a flip-flop connecting to either said second control end or said first control end;

a first pin connecting to said first data end;

a second pin connecting to said first control end and said flip-flop;

a third pin connecting to said second data end;

a fourth pin connecting to said first output end and said second output end.

Claim 18 (once amended):

18. A universal testing module [logic control unit] according to claim 17 wherein said flip-flop is [changed to connect] connected to said first control end.

Claim 19 (once amended):

19. A universal testing module [logic control unit] according to claim 17 wherein said first, second and third pin are selectively connected with a pull up resistor for stabilizing voltage when any of said pins is open.

Claim 20 (once amended):

20. A universal testing module [logic control unit] according to claim 17 wherein said first,